

SANYO Semiconductors DATA SHEET

An ON Semiconductor Company

LB11946 — PWM Current Control Stepping Motor Driver

Overview

The LB11946 is a stepping motor driver IC that implements PWM current control bipolar drive with a fixed off time. This IC features 15 current setting levels using a fixed VREF voltage and support for micro-stepping drive from 1-2 phase excitation drive to 4W1-2 phase excitation drive. This device is optimal for driving stepping motors such as those used for carriage drive and paper feed in printers.

Features

- PWM current control (with a fixed off time)
- Logic input serial-parallel converter (allows 1-2, W1-2, 2W1-2, and 4W1-2 phase excitation drive)
- Current attenuation switching function (with slow decay, fast decay, and mixed decay modes)
- Built-in upper and lower side diodes
- Simultaneous on state prevention function (through current prevention)
- Noise canceller function
- Thermal shutdown circuit
- Shutoff on low logic system voltage circuit
- Low-power mode control pin

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Motor supply voltage	V _{BB}		50	V
Peak output current	I _O peak	$tw \le 20 \mu S$	1.2	Α
Continuous output current	I _O max		1.0	Α
Logic system supply voltage	VCC		7.0	V
Logic input voltage range	V _{IN}		-0.3 to V _{CC}	V
Emitter output voltage	VE	V _{CC} = 5V specifications	1.0	V
		V _{CC} = 3.3V specifications	0.5	V
Allowable power dissipation	Pd max	Independent IC	3.0	W
Operating temperature	Topr		-25 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

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Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Motor supply voltage	V _{BB}		10 to 45	V
Logic system supply voltage	VCC	V _{CC} = 5V specifications	4.5 to 5.5	V
		V _{CC} = 3.3V specifications	3.0 to 3.6	V
Reference voltage	VREF	V _{CC} = 5V specifications	0.0 to 3.0	V
		V _{CC} = 3.3V specifications	0.0 to 1.0	V

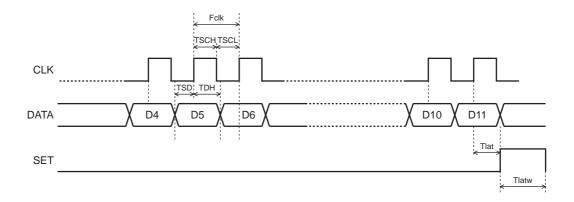
Electrical Characteristics at Ta = 25°C, $V_{CC} = 5V$, $V_{BB} = 42V$, VREF = 1.52V

Parameter	Symbol	Conditions		Unit			
i didilicici	Cyllibol	Conditions	min	typ	max	Jim	
Output Block							
Output stage supply current	I _{BB} ON		0.9	1.3	1.7	mA	
	I _{BB} OFF		0.52	0.7	1.05	mA	
Output saturation voltage	V _O (sat) 1	$I_O = +0.5A \text{ (sink)}$		1.1	1.4	٧	
	V _O (sat) 2	$I_O = +1.0A \text{ (sink)}$		1.4	1.7	٧	
	V _O (sat) 3	I _O = -0.5A (source)		1.9	2.2	٧	
	V _O (sat) 4	I _O = -1.0A (source)		2.2	2.5	V	
Output leakage current	I _O 1 (leak)	$V_O = V_{BB}$ (sink)			50	μΑ	
	I _O 2 (leak)	V _O = 0V (source)	-50			μΑ	
Output sustain voltage	V _{SUS}	L = 15mH, I _O = 1.0A, Design guarantee *	45			V	
Logic Block							
Logic system supply current	I _{CC} ON	D0 = 1, D1 = 1, D2 = 1, D3 = 1 When these data values are set	24	35	46	mA	
	I _{CC} OFF1	D0 = 0, D1 = 0, D2 = 0, D3 = 0	22	32	42	mA	
	I _{CC} OFF2	ST = LOW		0.05	0.1	mA	
Input voltage	V _{IH}		2			V	
	V _{IL}				0.8	V	
Input current	lН	V _{IH} = 2 V			35	μΑ	
	I _{IL}	V _{IL} = 0.8 V	6			μΑ	
Sense voltages	VE	D0 = 1, D1 = 1, D2 = 1, D3 = 1 When these data values are set	0.470	0.50	0.525	V	
		D0 = 1, D1 = 1, D2 = 1, D3 = 0	0.445	0.48	0.505	V	
		D0 = 1, D1 = 1, D2 = 0, D3 = 1	0.425	0.46	0.485	V	
		D0 = 1, D1 = 1, D2 = 0, D3 = 0	0.410	0.43	0.465	V	
		D0 = 1, D1 = 0, D2 = 1, D3 = 1	0.385	0.41	0.435	V	
		D0 = 1, D1 = 0, D2 = 1, D3 = 0	0.365	0.39	0.415	V	
		D0 = 1, D1 = 0, D2 = 0, D3 = 1	0.345	0.37	0.385	V	
		D0 = 1, D1 = 0, D2 = 0, D3 = 0	0.325	0.35	0.365	V	
		D0 = 0, D1 = 1, D2 = 1, D3 = 1	0.280	0.30	0.325	V	
		D0 = 0, D1 = 1, D2 = 1, D3 = 0	0.240	0.26	0.285	V	
		D0 = 0, D1 = 1, D2 = 0, D3 = 1	0.195	0.22	0.235	V	
		D0 = 0, D1 = 1, D2 = 0, D3 = 0	0.155	0.17	0.190	V	
		D0 = 0, D1 = 0, D2 = 1, D3 = 1	0.115	0.13	0.145	V	
		D0 = 0, D1 = 0, D2 = 1, D3 = 0	0.075	0.09	0.100	V	
Reference current	I _{REF}	VREF = 1.5V	-0.5			μА	
CR pin current	ICR	CR = 1.0V	-1.6	-1.2	-0.8	mA	
MD pin current	I _{MD}	MD = 1.0V, CR = 4.0V	-5.0			μА	
Logic system on voltage	V _{LSD} ON		2.6	2.8	3.0	V	
Logic system off voltage	V _{LSD} OFF		2.45	2.65	2.85	V	
LVSD hysteresis	VLHIS		0.03	0.15	0.35	V	
Thermal shutdown temperature		Design guarantee *		170		°C	

^{*}Design guarantee: Design guarantee value, Do not measurement.

AC Electrical Characteristics at $V_{CC} = 5V$

Parameter	Cumbal	Conditions		Unit			
Parameter	Symbol	Conditions	min	typ	max	Offic	
Clock frequency	Fclk			200	550	kHz	
Data setup time	TDS		0.9	2.5		μS	
Data hold time	TDH		0.9	2.5		μS	
Minimum clock high-level pulse width	TSCH		0.9	2.5		μS	
Minimum clock low-level pulse width	TSCL		0.9	2.5		μS	
SET pin stipulated time	Tlat		0.9	2.5		μS	
SET pin signal pulse width	Tlatw		1.9	5.0		μS	



$\textbf{Electrical Characteristics} \ at \ Ta = 25^{\circ}C, \ V_{CC} = 3.3V, \ V_{BB} = 42V, \ VREF = 1.0V$

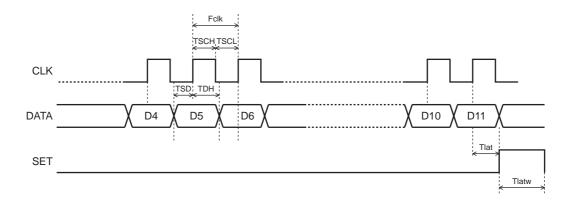
(When measuring the sense voltage: VREF = 1.03V)

Parameter	Symbol	Conditions		Ratings		Unit
raiametei	Symbol	Conditions	min	typ	max	Offic
Output Block						
Output stage supply current	I _{BB} ON		0.9	1.3	1.7	mA
	I _{BB} OFF		0.52	0.7	1.05	mA
Output saturation voltage	V _O (sat) 1	$I_O = +0.5A \text{ (sink)}$		1.2	1.5	٧
	V _O (sat) 2	$I_O = +1.0A \text{ (sink)}$		1.5	1.8	V
	V _O (sat) 3	I _O = -0.5A (source)		2.0	2.3	V
	V _O (sat) 4	I _O = -1.0A (source)		2.3	2.6	٧
Output leakage current	I _O 1 (leak)	$V_O = V_{BB}$ (sink)			50	μΑ
	I _O 2 (leak)	V _O = 0V (source)	-50			μА
Output sustain voltage	V _{SUS}	L = 15mH I _O -1.5A, Design guarantee *	45			V
Logic Block	•			•		
Logic system supply current	ICC ON	D0 = 1, D1 = 1, D2 = 1, D3 = 1	21	30	39	mΛ
		When these data values are set				mA
	I _{CC} OFF1	D0 = 0, D1 = 0, D2 = 0, D3 = 0	19	28	36.5	mA
	I _{CC} OFF2	ST = 0.8V		0.03	0.1	mA
Input voltage	VIH		2			V
	V _{IL}				0.8	V
Input current	lн	V _{IH} = 2V			35	μА
	IIL	V _{IL} = 0.8V	6			μА
Sense voltages	VE	D0 = 1, D1 = 1, D2 = 1, D3 = 1 VREF = 1.03V	0.303	0.330	0.356	٧
		D0 = 1, D1 = 1, D2 = 1, D3 = 0 VREF = 1.03V	0.290	0.315	0.341	V
		D0 = 1, D1 = 1, D2 = 0, D3 = 1 VREF = 1.03V	0.276	0.300	0.324	V
		D0 = 1, D1 = 1, D2 = 0, D3 = 0 VREF = 1.03V	0.263	0.286	0.309	V
		D0 = 1, D1 = 0, D2 = 1, D3 = 1 VREF = 1.03V	0.250	0.272	0.294	V
		D0 = 1, D1 = 0, D2 = 1, D3 = 0 VREF = 1.03V	0.236	0.257	0.278	٧
		D0 = 1, D1 = 0, D2 = 0, D3 = 1 VREF = 1.03V	0.223	0.243	0.263	V
		D0 = 1, D1 = 0, D2 = 0, D3 = 0 VREF = 1.03V	0.209	0.228	0.247	V
		D0 = 0, D1 = 1, D2 = 1, D3 = 1 VREF = 1.03V	0.183	0.200	0.217	V
		D0 = 0, D1 = 1, D2 = 1, D3 = 0 VREF = 1.03V	0.155	0.170	0.185	V
		D0 = 0, D1 = 1, D2 = 0, D3 = 1 VREF = 1.03V	0.128	0.143	0.158	V
		D0 = 0, D1 = 1, D2 = 0, D3 = 0 VREF = 1.03V	0.102	0.114	0.126	V
		D0 = 0, D1 = 0, D2 = 1, D3 = 1 VREF = 1.03V	0.074	0.085	0.096	V
		D0 = 0, D1 = 0, D2 = 1, D3 = 0 VREF = 1.03V	0.047	0.057	0.067	V
Reference current	I _{REF}	VREF = 1.0V	-0.5			μА
CR pin current	ICR	CR = 1.0V	-0.91	-0.7	-0.49	mA
MD pin current	I _{MD}	MD = 1.0V, CR = 4.0V	-5.0			μΑ
LVSD voltage	V _{LSD} ON		2.6	2.8	3.0	V
Logic system off voltage	V _{LSD} OFF		2.45	2.65	2.85	V
LVSD hysteresis	V _{LHIS}		0.03	0.15	0.35	V
Thermal shutdown temperature	Ts	Design guarantee *		170		°C

 $[\]ensuremath{^{*}\text{Design}}$ guarantee: Design guarantee value, Do not measurement.

AC Electrical Characteristics at $V_{CC} = 3.3V$

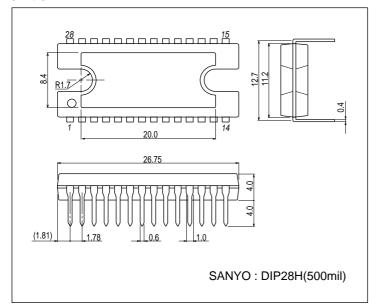
Parameter	Cumphal	Conditions		Ratings	Unit		
Parameter	Symbol	Conditions	min	typ	max	Offic	
Clock frequency	Fclk			200	550	kHz	
Data setup time	TDS		0.9	2.5		μS	
Data hold time	TDH		0.9	2.5		μS	
Minimum clock high-level pulse width	TSCH		0.9	2.5		μS	
Minimum clock low-level pulse width	TSCL		0.9	2.5		μS	
SET pin stipulated time	Tlat		0.9	2.5		μS	
SET pin signal pulse width	Tlatw		1.9	5.0		μS	

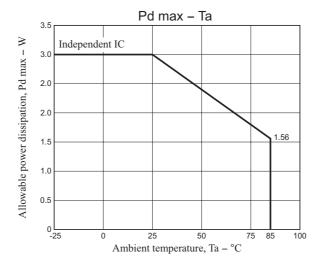


Package Dimensions

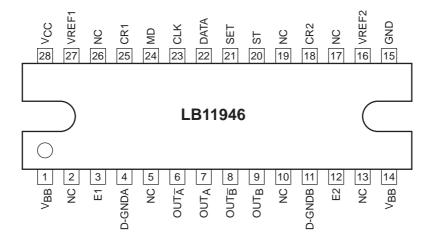
unit: mm (typ)

3147C



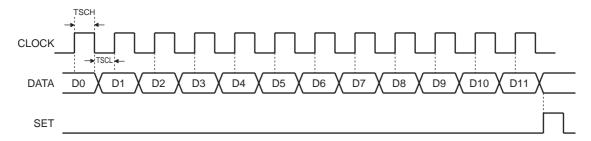


Pin Assignment



Note: The D-GNDA and D-GNDB pins are the anode sides of the lower side diodes

Timing Chart



Serially Transferred Data Definition

	IA4	IA3	IA2	IA1	DE1	PH1	IB4	IB3	IB2	IB1	DE2	PH2		Output	mode		I/O	DEC
No.	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	OUT_A	OUTA	OUTB	OUTB	ratio	MODE
0	1	1	1	1	1	1	1	1	1	1	1	1	Н	L	Н	L	100%	SLOW
1	1	1	1	0	1	1	1	1	1	0	1	1	Н	L	Н	L	96	SLOW
2	1	1	0	1	1	1	1	1	0	1	1	1	Н	L	Н	L	91	SLOW
3	1	1	0	0	1	1	1	1	0	0	1	1	Н	L	Н	L	87	SLOW
4	1	0	1	1	1	1	1	0	1	1	1	1	Н	L	Η	L	83	SLOW
5	1	0	1	0	1	1	1	0	1	0	1	1	Н	L	Η	L	78	SLOW
6	1	0	0	1	1	1	1	0	0	1	1	1	Н	L	Η	L	74	SLOW
7	1	0	0	0	1	1	1	0	0	0	1	1	Н	L	Н	L	70	SLOW
8	0	1	1	1	1	1	0	1	1	1	1	1	Н	L	Н	L	61	SLOW
9	0	1	1	0	1	1	0	1	1	0	1	1	Н	L	Н	L	52	SLOW
10	0	1	0	1	1	1	0	1	0	1	1	1	Н	L	Н	L	44	SLOW
11	0	1	0	0	1	1	0	1	0	0	1	1	Н	L	Н	L	35	SLOW
12	0	0	1	1	1	1	0	0	1	1	1	1	Н	L	Н	L	26	SLOW
13	0	0	1	0	1	1	0	0	1	0	1	1	Н	L	Н	L	17	SLOW
14	1	1	1	1	0	0	1	1	1	1	0	0	L	Н	L	Н	100	FAST
15	1	1	1	0	0	0	1	1	1	0	0	0	L	Н	L	Н	96	FAST
16	1	1	0	1	0	0	1	1	0	1	0	0	L	Н	L	Н	91	FAST
17	1	1	0	0	0	0	1	1	0	0	0	0	L	Н	L	Н	87	FAST
18	1	0	1	1	0	0	1	0	1	1	0	0	L	Н	L	Н	83	FAST
19	1	0	1	0	0	0	1	0	1	0	0	0	L	Н	L	Н	78	FAST
20	1	0	0	1	0	0	1	0	0	1	0	0	L	Н	L	Н	74	FAST
21	1	0	0	0	0	0	1	0	0	0	0	0	L	Н	L	Н	70	FAST
22	0	1	1	1	0	0	0	1	1	1	0	0	L	Н	L	Н	61	FAST
23	0	1	1	0	0	0	0	1	1	0	0	0	L	Н	L	Н	52	FAST
24	0	1	0	1	0	0	0	1	0	1	0	0	L	Н	L	Н	44	FAST
25	0	1	0	0	0	0	0	1	0	0	0	0	L	Н	L	Н	35	FAST
26	0	0	1	1	0	0	0	0	1	1	0	0	L	Н	L	Н	26	FAST
27	0	0	1	0	0	0	0	0	1	0	0	0	L	Н	L	Н	17	FAST
28	0	0	0	0	*	*	0	0	0	0	*	*	OFF	OFF	OFF	OFF	0	-

Note *: Either 0 or 1.

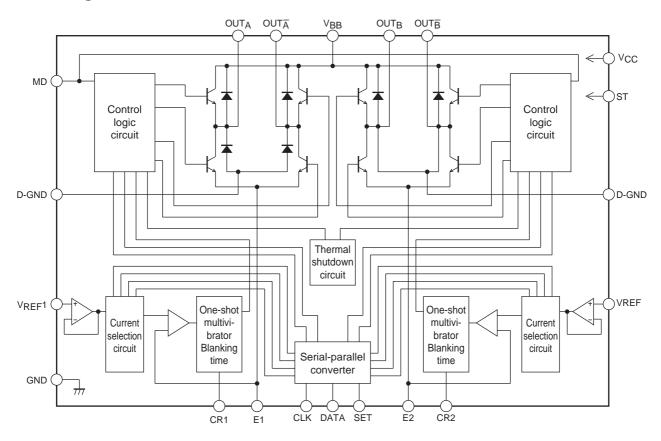
Note $^{\star}1$: In mixed decay mode, set D4 and D10 to 0 and set the MD pin to a level in the range 1.5 to 4.0V.

Current Settings Truth Table * Items in parentheses are defined by the serial data.

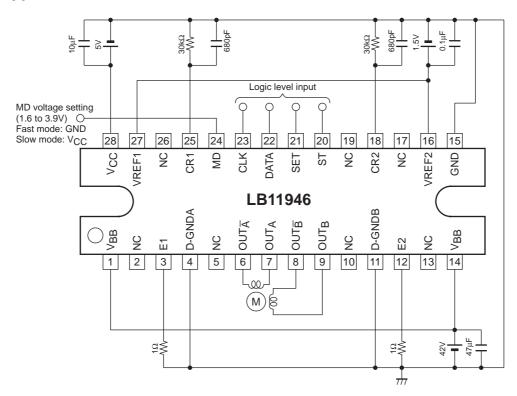
IA4 (D0)	IA3 (D1)	IA2 (D2)	IA1 (D3)	Set current lout	Current ratio (%)
1	1	1	1	11.5/11.5 × VREF/3.04RE = lout	100
1	1	1	0	11.0/11.5 × VREF/3.04RE = lout	95.65
1	1	0	1	10.5/11.5 × VREF/3.04RE = lout	91.30
1	1	0	0	10.0/11.5 × VREF/3.04RE = lout	86.95
1	0	1	1	9.5/11.5 × VREF/3.04RE = lout	82.61
1	0	1	0	9.0/11.5 × VREF/3.04RE = lout	78.26
1	0	0	1	8.5/11.5 × VREF/3.04RE = lout	73.91
1	0	0	0	8.0/11.5 × VREF/3.04RE = lout	69.56
0	1	1	1	7.0/11.5 × VREF/3.04RE = lout	60.87
0	1	1	0	6.0/11.5 × VREF/3.04RE = lout	52.17
0	1	0	1	5.0/11.5 × VREF/3.04RE = lout	43.48
0	1	0	0	4.0/11.5 × VREF/3.04RE = lout	34.78
0	0	1	1	3.0/11.5 × VREF/3.04RE = lout	26.08
0	0	1	0	2.0/11.5 × Vref/3.04RE = lout	17.39

Note: The current ratios shown are calculated values.

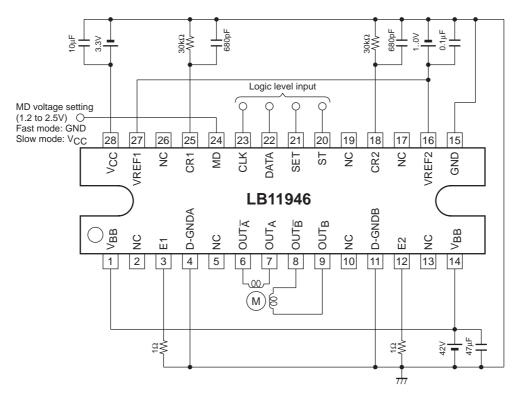
Block Diagram



Sample Application Circuit at $V_{CC} = 5V$



Sample Application Circuit at $V_{CC} = 3.3V$



SLOW DECAY Current Path

The reregenerative current at upper-side transistor switching operates

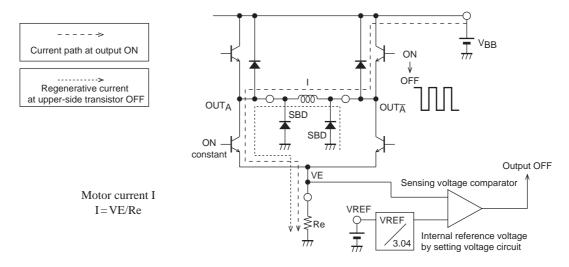


Fig.1

FAST DECAY Current Path

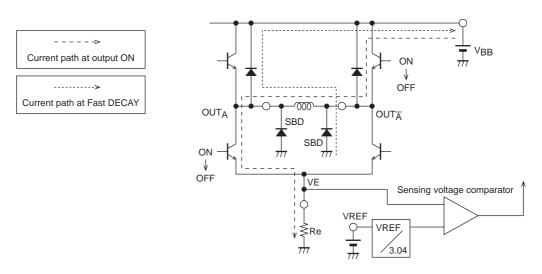
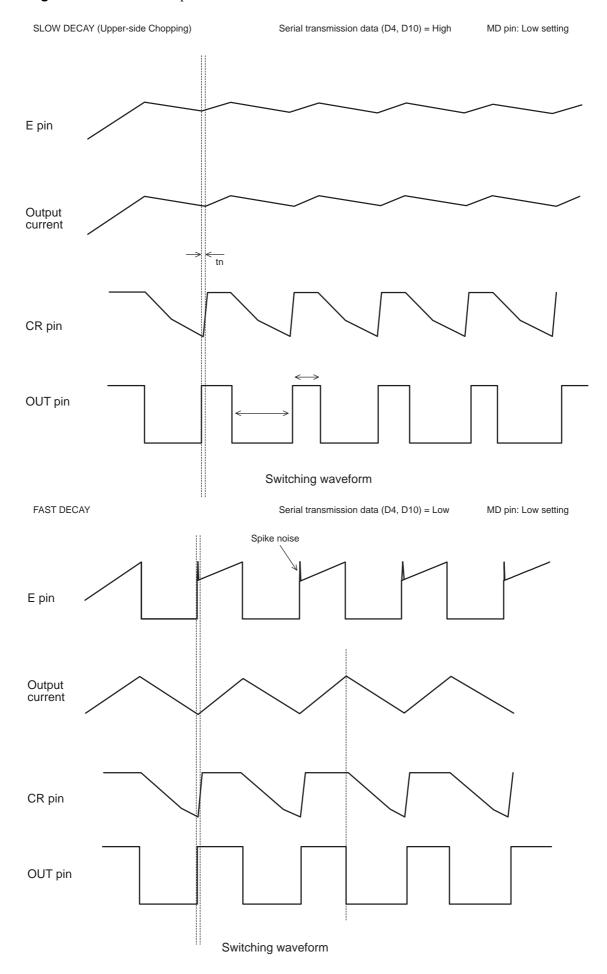
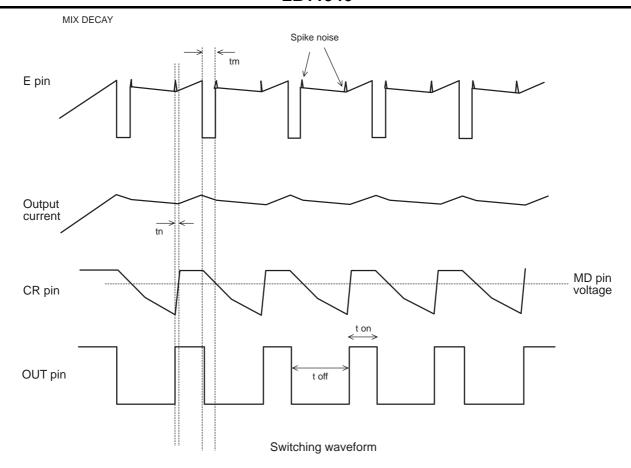


Fig.2

Switching Time Chart at PWM operation





MIX DECAY logic setting

serial transmission data (D4, D10) = Low

MD pin: 1.6V to 3.0V at $V_{CC} = 5V$ specification.

1.2V to 2.5V at $V_{CC} = 3.3V$ specification.

t on: Output ON time

t off: Output OFF time

tm: FAST DECAY time at MIX DECAY mode

tn: Noise cancel time

The following operation by comparison between CR voltage and MD pin voltage in turning off time.

CR voltage > MD pin voltage: both sides chopping

CR voltage < MD pin voltage: upper side chopping

Attached Documents

1. Switching Off Time and Noise Canceller Time Calculations

Notes on the CR Pin Setting (switching off time and noise canceller time)

The noise canceller time (Tn) and the switching off time (Toff) are set using the following formulas.

(1) When VCC is 5 V

Noise canceller time (Tn)

$$Tn \approx C \times R \times ln \{(1.5 - RI) / (4.0 - RI)\}[s]$$

CR pin charge current: 1.25mA

Switching off time (Toff)

Toff
$$\approx$$
 -C × R × ln (1.5/4.8)[s]

Component value ranges

R: $5.6k\Omega$ to $100k\Omega$ C: 470pF to 2000pF

(2) When V_{CC} is 3.3 V

Noise canceller time (Tn)

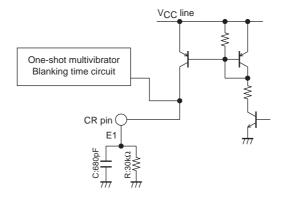
$$Tn \approx C \times R \times ln \{(1.06 - RI) / (2.66 - RI)\}[s]$$

CR pin charge current: 0.7 mA

Switching off time (Toff)

Toff
$$\approx$$
 -C \times R \times ln $(1.06 / 3.1)[s]$

CR Pin Internal Circuit Structure



- 2. Notes on the MD Pin
- (1) If slow decay mode is set up by setting the D4 and D10 bits in the input serial data to 1, the MD pin must be shorted to ground.
- (2) If fast decay mode is set up by setting the D4 and D10 bits in the input serial data to 0, mixed decay mode can be set with the MD pin.

When the $V_{CC} = 5V$ specifications are used the setting voltage range for mixed decay mode is 1.6 to 3.9V.

When the $V_{CC} = 3.3V$ specifications are used the setting voltage range for mixed decay mode is 1.2 to 2.5V.

If mixed decay mode will not be used with the fast decay mode setting, either:

- (a) Short the MD pin to ground to select fast decay mode, or
- (b) Short the MD pin to V_{CC} to select slow decay mode.

Usage Notes

(1) Notes on the VREF pin

Since the VREF pin inputs the reference voltage used to set the current, applications must be designed so that noise does not occur at this pin.

(2) Notes on the ground pins

Since this IC switches large currents, care is required with respect to the ground pins.

The PCB pattern in sections where large currents flow must be designed with low impedances and must be kept separate from the small-signal system.

In particular, the ground terminals of the E1 and E2 pin sense resistors (Re) and the external Schottky barrier diode ground terminals must be located as close as possible to the IC ground. The capacitors between V_{CC} and ground and between V_{BB} and ground must be as close as possible to the corresponding V_{CC} and V_{BB} pin in the pattern.

(3) Power on sequence

When turning the power systems on

 $V_{CC} \rightarrow logic \ level \ inputs \ (CLK, DATA, SET, and ST) \rightarrow VREF \rightarrow V_{BB}$

When turning the power systems off

 $V_{BB} \rightarrow V_{REF}$ logic level inputs (CLK, DATA, SET, and ST) $\rightarrow V_{CC}$

Note that if the power supply for the logic level inputs is on when the V_{CC} power supply is off, a bias with an unstable state will be applied due to the protection diodes at the V_{CC} pins, and this can cause incorrect operation.

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